RECEIVED
CENTRAL FAX CENTER
NOV 17 2006

REMARKS

Claims 4 and 13 have been canceled, and Claims 1 and 10 have been amended. Claims 1-3, 5-12 and 14-18 are currently pending in the application. In view of the remarks that follow, Applicants respectfully request reconsideration.

Independent Claim 10

Claim 10 recited two different "insulator" layers. In order to ensure a clear antecedent relationship between the original recitation of each "insulator" layer and subsequent references to it, Claim 10 (and dependent Claims 16-18) have been amended to refer to one of these layers as a "further" insulator layer. These modifications do not affect the intended scope of Claims 10-12 and 14-18.

With reference to the Office Action mailed on September 20, 2006, independent Claim 10 was rejected under 35 U.S.C. §102 as anticipated by Ma U.S. Patent No. 6,025,242. However, in view of the foregoing amendments to Claim 10, it is respectfully submitted that Claim 10 is distinct from Ma. In more detail, the PTO specifies in MPEP §2131 that, in order for a reference to anticipate a claim under §102, the reference must teach each and every element recited in the claim. Claim 10 recites:

> A method of forming a semiconductor device on a semiconductor substrate featuring a high dielectric constant (high k) gate insulator layer, comprising the steps of:
>
> forming said high k gate insulator layer on said semiconductor substrate, said high k gate insulator layer having a dielectric constant greater than the dielectric constant of silicon oxide;

> forming a conductive gate structure overlying a first area of said high k gate insulator layer;
>
> depositing a further insulator layer;
>
> performing a dry etch procedure to first define first insulator spacers on the sides of said conductive gate structure via etching of said further insulator layer, and then to remove exposed portions of said high k gate insulator layer, wherein said exposed portions of said high k gate insulator layer are portions not covered by said conductive gate structure or by said first insulator spacers; . . . .

As explained in the "Description of Prior Art" section on pages 1-2 of the present application, the semiconductor device fabrication industry has moved toward the use of transistor gate dielectrics that have a relatively high dielectric constant "k", and that are commonly referred to as "high-k" dielectric materials. As also explained on pages 1-2, standard dielectric materials (such as silicon oxide) can be removed from a device much more easily than high-k dielectric materials. In fact, the traditional process for removing a standard dielectric such as silicon oxide is not fully effective to remove a high-k dielectric. Consequently, an expensive additional process step has traditionally been needed in order to remove unwanted portions of a high-k gate dielectric layer before source/drain formation. As discussed on page 2 of the present application, Applicants have developed a device fabrication procedure where a high-k material is used as a gate dielectric, but where unwanted portions of that high-k layer are removed without the need to use the additional and expensive process step. A further consideration is that, if the high-k gate dielectric layer is removed after the first insulator spacers are formed, the short channel effect of the resulting transistor is improved.

The §102 rejection of Claim 10 is based on the embodiment shown in Figures 1-6 of the Ma patent, where a gate dielectric layer 2 is made of silicon oxide (lines 21-23 in column 2). It is

well-known in the art that silicon oxide is not a high-k material, and there is nothing in Ma that states the layer 2 is considered to be high-k. In the last line on page 6 of the Office Action, the Examiner asserts that Applicants consider silicon oxide to be a high-k material, based on a sentence that appeared at lines 7-9 on page 5 of Applicants' originally-filed specification. However, a prior Response has already corrected the obvious error in that sentence, because the reference there to silicon oxide was not consistent with common knowledge in the art, and was also not consistent with other portions of the present application. For example, a sentence at lines 11-13 on page 1 of Applicant's specification reflects the common understanding that silicon oxide is not a high-k material, stating that "to maintain a thin gate insulator layer with reduced risk of leakage high k layers can be used in place of the lower k, silicon dioxide layers".

In the Advisory Action mailed on October 27, the Examiner notes that Chan U.S. Patent No. 6,380,088 states silicon oxide is a high-k material. However, Chan is not a reference of record, and it is not proper for the Examiner to start relying on new art in an Advisory Action. Further, the indicated statement in Chan is directly inconsistent with common knowledge in the industry, as well as statements in the present application, such as the above-quoted sentence in lines 11-13 on page 1, where Applicants state that "to maintain a thin gate insulator layer with reduced risk of leakage high k layers can be used in place of the lower k, silicon dioxide layers". Chan does not supersede this statement by Applicants that silicon oxide is not a high-k material. The rejection of Claim 10 is an anticipation rejection under §102 that is based solely on Ma. This means that Ma, by itself, must disclose the entirety of what is recited in Claim 10. But Ma does not do so.

In addition to the considerations discussed above, the foregoing amendments modify Claim 10 to add a phrase specifying "said high k gate insulator layer having a dielectric constant that is greater than the dielectric constant of silicon oxide". The silicon oxide layer of Ma clearly does not meet this limitation, with or without reference to Chan. Ma clearly fails to disclose each and every element that is recited in Applicants' Claim 10. Accordingly, Ma does not anticipate

Claim 10 under §102. Claim 10 is therefore believed to be allowable, and notice to that effect is respectfully requested.

Independent Claim 1

Independent Claim 1 recites:

> forming a high dielectric constant (high k) gate dielectric layer on said semiconductor substrate, said gate dielectric layer having a dielectric constant greater than the dielectric constant of silicon oxide;
>
> forming a conductive gate structure on a first area of said gate dielectric layer;
>
> forming first insulator spacers on the sides of said conductive gate structure with the procedure used to form said first insulator spacers also removing a second area of said gate dielectric layer, wherein said second area of said gate dielectric layer is not covered by said conductive gate structure or by said first insulator spacers; . . . .

Claim 1 stands rejected under 35 U.S.C. §102 as anticipated by the Ma patent. The rationale offered for the rejection of Claim 1 is similar to the rationale offered for the rejection of Claim 10. The foregoing amendments add to Claim 1 a phrase specifying "said gate dielectric layer having a dielectric constant that is greater than the dielectric constant of silicon oxide". For reasons similar to those discussed above in association with Claim 10, it is respectfully submitted that Claim 1 is patentably distinct from Ma, and notice to that effect is respectfully requested.

RECEIVED
CENTRAL FAX CENTER
NOV 17 2006

Dependent Claims

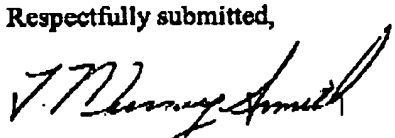
Claims 2-3 and 5-9, and Claims 11-12 and 14-18 respectively depend from Claim 1 and Claim 10, and are also believed to be distinct from the art of record, for example for the same reasons discussed above with respect to Claims 1 and 10.

Conclusion

Based on the foregoing, it is respectfully submitted that all of the pending claims are fully allowable, and favorable reconsideration of this application is therefore respectfully requested. If the Examiner believes that examination of the present application may be advanced in any way by a telephone conference, the Examiner is invited to telephone the undersigned attorney at 972-739-8647.

Although Applicants believe that no fee is due in association with the filing of this Response, the Commissioner is hereby authorized to charge any additional fee required by this paper, or to credit any overpayment, to Deposit Account No. 08-1394 of Haynes and Boone LLP.

Respectfully submitted,



T. Murray Smith
Registration No. 30,222
(972) 739-8647

Date: November 17, 2006

HAYNES AND BOONE, LLP
901 Main Street, Suite 3100
Dallas, Texas 75202-3789
Telephone: (972) 739-6900
Facsimile: (214) 200-0853
File: 24061.504

Enclosures: None

R-151502.1